Power and Memory Optimization in Low Power VLSI Design- A New Technique

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ABSTRACT
This paper proposes a new technique to low power approaches for very large scale integration (VLSI) design. Power dissipation is one of the major concerns when designing a VLSI system. Until recently, dynamic power was the only concern. However, as the technology feature size shrinks, static power, which was negligible before, becomes an issue as important as dynamic power. Since static power increases dramatically in nanoscale silicon VLSI technology, the importance of reducing leakage. This paper describes a novel low-leakage technique sleepy stack. The sleepy stack technique is applied to generic logic circuits, and achieve between two and three orders of magnitude leakage power reduction compared to the best prior state saving technique we could find (namely, the forced stack technique)power consumption cannot be overstressed.

KEYWORDS
Dual- V_{th}, low-leakage power dissipation, sleepy stack, transistor stacking.

INTRODUCTION

The increasing demand of portable system and restriction in power consumption in VLSI and ULSI has become an important and challenging point today. In 1980 s' CMOS took main stream in VLSI because it consumes far less power. This advantage still holds today but due to the recent growing demand in portable device transistor size has to be scale down and this will increase the power consumption. So, we will say that as the technology features scale down, as the sub-threshold increases, the power consumption in nanoscale VLSI increases which is a great problem today. Power consumption in CMOS is mainly due to dynamic and static power. Dynamic power consist switching power and short circuit power. Switching power is consumed when gate charges its output capacitance and short circuit power is consumed when both PMOS and NMOS turns on for an instance of time [1]. For 0.18µ technology and above dynamic power is major but below 0.18 µ technology by increasing value of sub-threshold leakage static power gives 90% contribution to power consumption. For nano-scale VLSI static power dissipation is the key design consideration. For high packing density requirement memory cells are packed with minimum feature size dimensions which are more sensitive to the impact of intrinsic device variation. More specifically threshold voltage variation in the memory circuit designs are of major concern because of the sensitivity of the read and write noise margins to the threshold voltage of neibouring transistor[3]. For scale down VLSI leakage current becoming a critical problem. Gate leakage in device has increased exponentially as oxide has reached a thickness of 3-4 atomic layers [4]. The thin insulation layer increases the tunneling leakage. This increase of leakage gives a huge power dissipation problem in memory cells in VLSI [2]. To avoid this power consumption problem we are presenting a novel circuit structure which we called 'sleepy-stack' that gives a sufficient way to reduce leakage power, but, with a delay increase. It dramatically reduces power consumption by using high Vt transistor while it also retains it state. Using sleepy-stack technique we get a excellent PDP factor and hence our goal achieves with low cost, low power sleepy stack technique with 150 nm scale.

BEFORE GOING STARTED

This paper is mainly focusing on reduction of leakage power in SRAM cell; hence here we include some important parameter dealing with it.

PDP Factor

The power delay product is a fundamental parameter which is often used for measuring the quality and the performance of a CMOS process and gate design. The more improved the PDP the more advanced VLSI system.

Leakage in SRAM

The sub-threshold leakage in 6-T SRAM can be categorized in two parts. (1) Cell leakage from supply to ground (2) Bit line leakage from bitline to ground.
When SRAM hold '0' i.e. in standby mode, the wordline signal is at logic '0' and bitlines are precharged at logic '1'. Zero state of the cell refers to the case when the storage node '1' is at logic '0' and storage node '0' is at logic '1'.

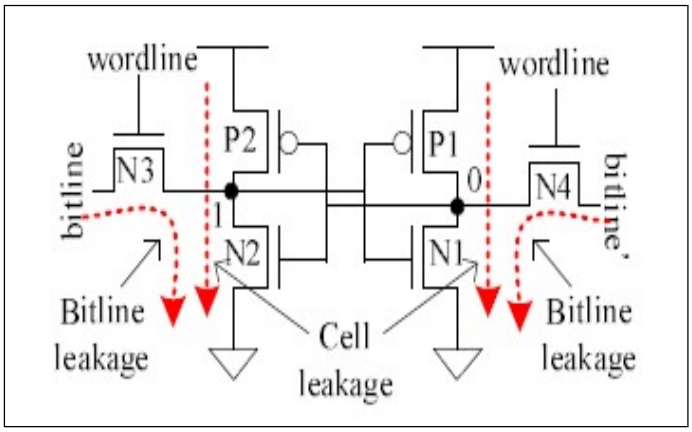

Fig. 1

For this case, the gate tunneling current of MOS transistors (N3/N4/N1/P2) in off state is much smaller. Typically, the gate tunneling current of a PMOS transistor (P1) is smaller as compared to NMOS transistor (N2) in on state, it is important to reduce gate leakage through transistor N2.

If an SRAM cell holds '1', the `bitline` leakage current passing through N3 and N2 is effectively suppressed due to two reasons. First, after precharging `bitline` and `bitline'` both to '1,' the source voltage and the drain voltage of N3 are the same, and thus potentially no current flows through N3. Second, two stacked and turned off transistors (N2 and N3) induce the stack effect. Meanwhile, for this case where the SRAM bit holds value '1,' a large `bitline'` leakage current flows passing through N4 and N1.

PREVIOUS RESEARCH FOR POWER REDUCTION

We can categorize previous research for leakage reduction technique by the following:

High Vt SRAM

This is the simplest way to reduce leakage for 6-T SRAM. By applying all high Vt transistor for 0.15 µ technology leakage power can be reduced. But the main disadvantage of it is increasing of delay to the system. This paper shows that using sleepy stack technique more power reduction is achieved and simultaneously a great PDP.

Sleep Transistor Technique

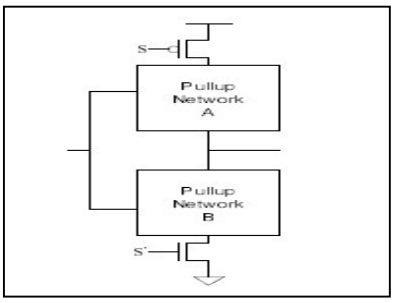

Fig. 2

Another technique for leakage reduction is sleep transistor technique which adds a pair of high Vt transistor between pull up and Vdd, and pull down and Gnd, while the logic circuit uses a low Vt transistors. The structural advantage is when the logic circuit is needed then only the sleep transistor are needed but when the logic circuit are not in use then the sleep transistors are goes into sleep mode i.e. turned off. So, by isolating the logic circuit the sleep transistor technique can reduce leakage in sleep mode. But, the problem is that it lost its state during sleep mode and hence to wake up it needs a significant value. In figure2 shows a sleep transistor technique.

Forced Stack Technique

Another technique is invoked later on which is called forced stack technique and which is still now the best state saving technique. It can reduce leakage current because of its structure. It divided each existing transistor into two half size of it with same input sharing. The following fig.3 shows a forces stack inverter structure with input A. When A=0, both M1 and M2 are turned off . When M1 and M2 are turning "off" both it raises the intermediate node voltage Vx to a positive value due to a small drain current. The positive Vx results a negative gate to source voltage (Vgs),a negative substrate bias voltage(Vsb) for M1.Thus M1 has negative drain to source voltage(Vds). These all effect gives a high rate leakage reduction [1]. But one disadvantage of forced stack is it can not use high Vt transistor while sleepy stack can use it.

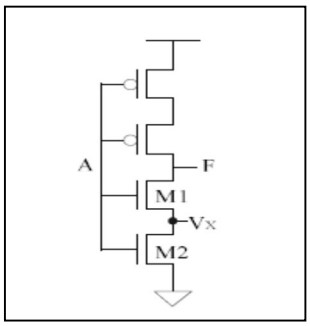

Fig. 3

SLEEPY STACK

To achieve ultra low leakage current sleepy stack is introduced. It has a combine structure of sleep transistor technique and forced stack technique. Unlike the sleep transistor technique sleepy stack technique can retain state and unlike forced stack technique sleepy stack technique can use high Vt transistors for power reduction. The following figure shows a sleepy stack inverter circuit. Here in the circuit have two combination structures. First, like the forced stack technique it divided each existing transistor into two half size of it and secondly it isolates the logic circuit using a pair of sleep transistor where we apply high Vt. The logic circuit uses low Vt transistors.

The operation of sleepy stack happens into two modes:

1. Active Mode

2. Sleep Mode

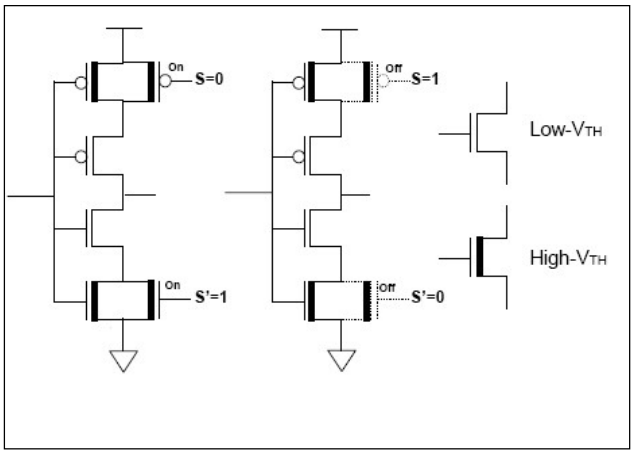

Fig. 4

The stacking effect of forced stack saves leakage power in sleep mode and sleep transistor achieve large leakage power saving using high Vt. The fig.4 shows sleepy stack inverter circuit in active and sleep mode. The sleep transistors are turned on during logic circuit operation (active mode) and turned off when it is not in use (sleep mode). During active mode when S=0 and S'=1 then all the sleep transistor turned on. The sleepy stack now can reduce circuit delay. As the sleep transistors are on during active mode then sleepy stack technique in active mode has a fast switching time. At each sleep transistor drain, the voltage value connected to the sleep transistor source is always ready and available at the sleep transistor drain, and thus the current flow is immediately available to the low Vt transistor connected to the gate output regardless of the status of each transistor in parallel to the sleep transistor. During sleep mode, S=1 and S=0 are asserted, and so both of the sleep transistors are turned off. Although the sleep transistors are turned off, the sleepy stack structure maintains exact logic state. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high - V_{TH} transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, two stacked and turned off transistors induce the stack effect, which also suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state [4].

SLEEPY STACK APPLIED ON SRAM CELL

We have done our experiment on 6-T SRAM cell which mainly consist of two inverter circuit and two word line transistor. We apply sleepy stack technique to the SRAM cell and we divided the circuit into sub parts for the propose of experiment. They are:

1. PU PD (pull up and pull down network).
2. PU WL (pull up and wordline network).
3. PD WL (pull down and wordline network).
4. PU PD WL (pull up, pull down and wordline network).

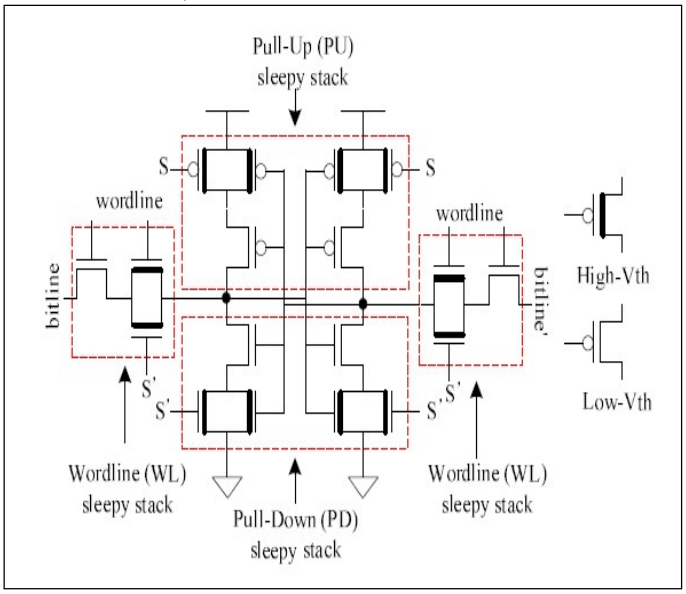

Fig. 5 – T Sleepy Stack SRAM Cell

The PD sleepy stack can suppress some part of the cell leakage. Meanwhile, the PU, PD sleepy stack can suppress the majority of the cell leakage. However, without applying the sleepy stack technique to the word line (WL) transistors, bitline leakage cannot be significantly suppressed. Although lying in the bitline leakage path, the pull-down sleepy stack is not effective to suppress both bitline leakage paths because one of the pull-down sleepy stacks is always on. Therefore, to suppress sub threshold leakage current in a SRAM cell fully, the PU, PD and WL sleepy stack approach needs to be considered [3].

SIMULATIONS AND RESULTS

We have done the simulation with 0.15µ technology with the help of TSPICE for low cost, low power design with good PDP. The supply voltage applied is 1V.

the simulation have done in three ways:

1. First we measure the power with base case i.e. conventional 6-T SRAM cell.
2. We then compare the base case with high Vt technique where all transistors are in high Vt.
3. Then we apply forced stack technique to the SRAM cell by dividing each transistor into two half size of it. All transistors are low Vt.
4. Finally we apply sleepy stack technique and measure power in four combination i.e. PU PD, PU WL, PD WL, PU PD WL.

The simulation result shows that using Sleepy stack technique the leakage reduction is maximized. It can reduce _% power compared to the best previous state saving technique, forced stack.

Table – 1

Result of SRAM cell

SL No.	Method	Power
1	Base Case	1419.6E-009
2	SRAM with high Vt	495.5E-009
3	SRAM with forced stack	25.204E-009
5	SRAM with sleepy stack	8.90E-009

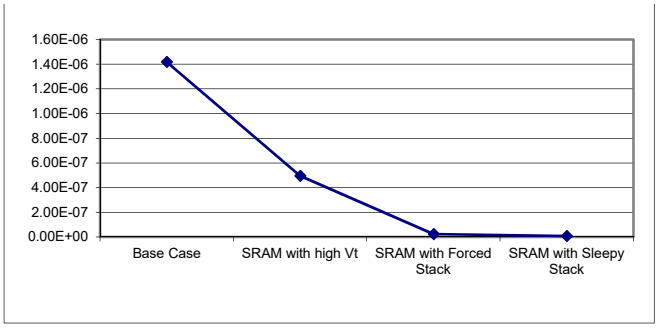

Fig. 6 simulation result

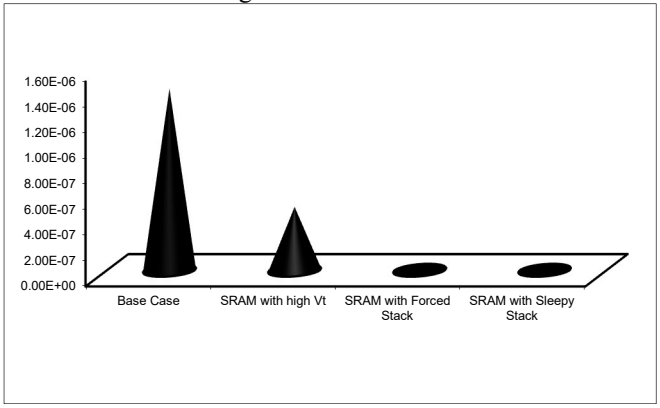

Fig. 7 simulation result

CONCLUSION

In sub-0.1µ- m CMOS technology, sub threshold leakage power consumption can be nearly equal to dynamic power consumption; thus, effective handling of leakage power is a great challenge. In this paper, we present a new circuit structure named "sleepy stack" to help tackle the leakage problem. The sleepy stack has a combined structure of two well-known low-leakage techniques: the forced stack and sleep transistor techniques. However, unlike the forced stack technique, the sleepy stack technique can utilize high- transistors without incurring large delay overhead. Also, unlike the sleep transistor technique, the sleepy stack technique can retain exact logic state while achieving similar leakage power savings. In short, our sleepy stack structure achieves ultra-low leakage power consumption while retaining state. We have explored a high-impact and heavily researched area: low-power VLSI design. The sleepy stack has been shown to have significant impact.

FUTURE SCOPE

This current work is a simulation approach towards understanding the performance possibilities. Further work is required in specific areas to more completely understand the limitations of the silicon-on-insulator approach for multi-gate devices since fabricating these devices on an individual basis for research purposes entail heavy investments a viable alternative to further explore device performance would be to make use of 3D process simulation programs that replicate the fabrication sequences and thereby help understand the sensitivities of the fabrication process in modifying device performance. This would definitely help in developing a better insight into device design as device dimensions, especially the gate length continue to shrink.

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